Mass production of Silicon MOS-SETs: Can we live with nano-devices' variability?

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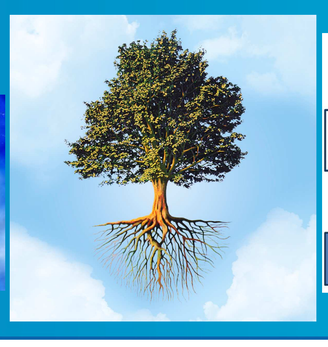
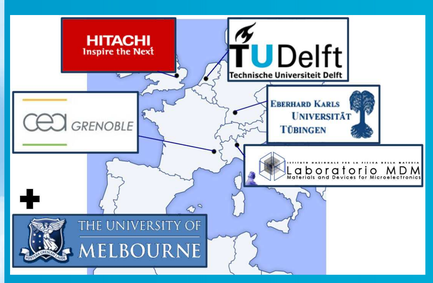
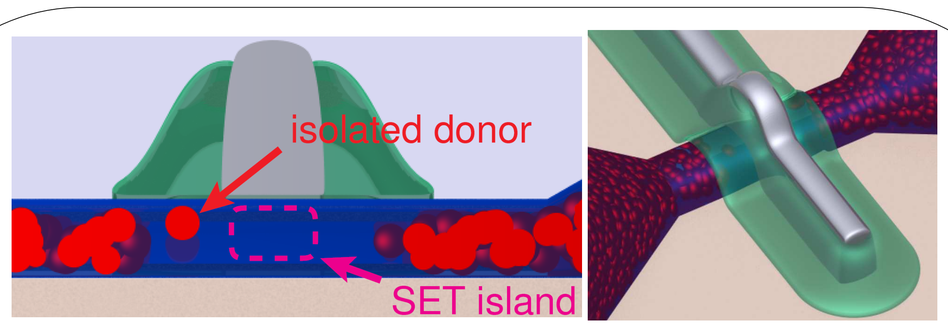




ABSTRACT

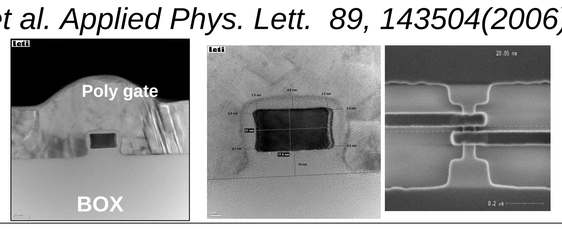
It is very important to study variability of nanodevices because the inability to produce large amounts of identical nanostructures is eventually a bottleneck for any application. In fact variability is already a major concern for CMOS circuits. In this work we report on the variability of dozens of silicon single-electron transistors (SETs). At room temperature their variability is compared with the variability of the most advanced CMOS FET i.e. the ultra thin Silicon-on-Insulator Multiple gate FET (UT SOI MuGFET). We found that dopants diffused from Source –Drain into the edge of the undoped channel are the main source of variability. This emphasizes the role of extrinsic factors like the contact junctions or the gate stack architectures and imperfections for variability of any nanodevice.



Layout for the MOS-SET: the SOI nanowire is in blue with HDD Arsenic donors as red spheres. The gate is in gray with the self aligned Si_3N_4 spacers in green. SOI cross section varies between 8×30nm² and 20×800nm², Gate length between 20 and 100nm, spacer width between 15 and 45 nm [V. N. Golovach et al. , Phys. Rev. B83, 075401 (2011)].

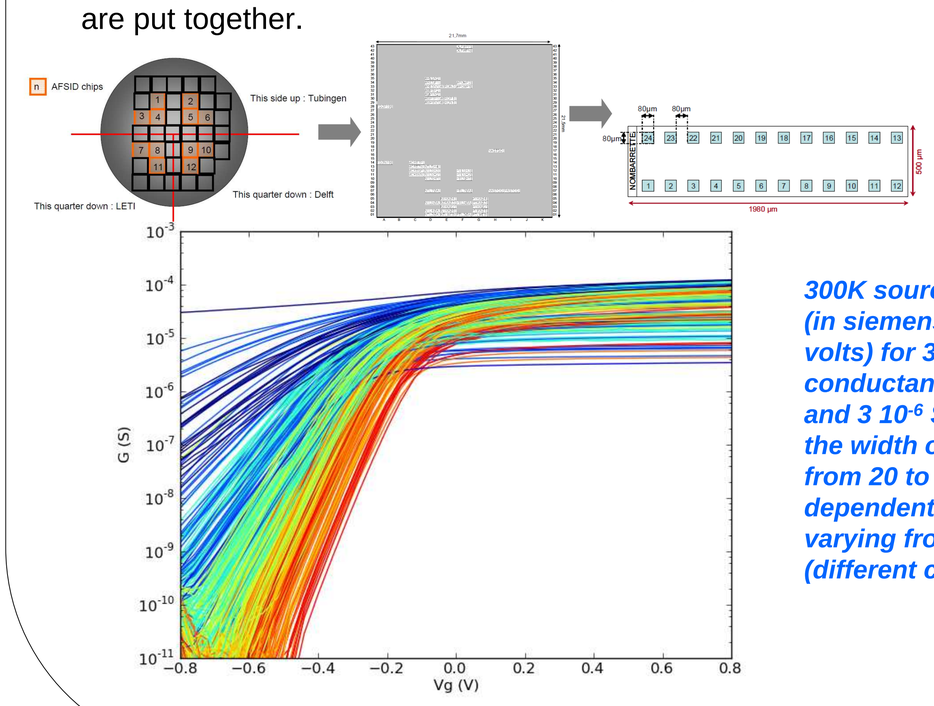
We fabricated silicon CMOS SETs starting from the UT SOI MuGFET geometry, with the goal to make very compact structures (10nm contact separation) with excellent gate control (i.e. large transconductance, large subthreshold swing (SS)). Thanks to the small Source-Drain separation and the small gate capacitance our devices show a delay time of about 2ps for Vds=1V at 300K. To be relevant for variability studies we consider a very simple design which is as close as possible to the optimized UT SOI MuGFET. The basic design is a crossbar geometry where a nanowire (NW) active SOI is covered by a perpendicular nanowire gate. Two spacers are formed on the edges of the gate. The gate and spacers are used as a mask for High Dose Doping (HDD) source-drain implantation (Low Dose Doping implantation can be performed in between). This way we realized a compact, simple, controllable MOS-SET

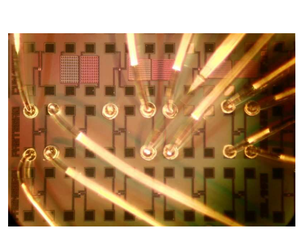
M. Hofheinz et al. Applied Phys. Lett. 89, 143504(2006).



MASS FABRICATION

In one batch we produced seventeen 200mm-wafers with various technological splits. In total 19584 single gated MOS-SETs, 14484 two-gated MOS-SETs, 1632 three-gated MOS-SETs and 816 four-gated MOS-SETs were produced.
The samples are probed electrically at room temperature using an automated probe station. I-V room temperature characteristics were fully recorded for 8160 single gate MOS-SETs. The samples are dispatched between 6 academic labs after these tests. They are cut, shipped, bonded, tested a second time at room temperature and then cooled down (to characterize SET behavior). An excellent yield is observed, permitting us to address the variability issue. An example of collected data on a large series of samples is presented below, where curves corresponding to samples with identical SOI thickness(20nm) but with different widths and lengths are put together.





300K source-drain conductance (in siemens) vs gate voltage (in volts) for 383 samples. ON-state conductance varies between 10^{-4} and 3 10^{-6} S @ 300K depending on the width of the channel ranging from 20 to 100nm. SS is strongly dependent on the gate length varying from 30 to 100 nm (different colours).

VARIABILITY

We found that dopants diffused from the highly arsenic doped Source –Drain (HDD) into the edge of the undoped channel (those below the nitride spacers on figure above) form the main source of variability *[R. Wacquez, et al., 2010 Symposium on VLSI technology, June 15-17, 2010 Honolulu , proceedings pp. 193-194; M. Pierre , R. Wacquez, X. Jehl, and M. Sanquer, Vinet and O. Cueto , Nature Nanotechnology 5, 133 - 137 (2010)].* This is valid both at room temperature (FET regime, above and below the threshold voltage) or at low temperature (SET regime). At low temperature the devices worked in the single electron transistor (SET) regime. Dopants diffused from HDD are the main cause of variability and they impact both the amplitude and the phase of the SET oscillations: the former effect comes from their influence on the energy dependence of the tunnelling rate for carriers, the later effects is due to their influence as offset charges *[M. Hofheinz, X. Jehl, and M. Sanquer G. Molas, M. Vinet, and S. Deleonibus, European Phys. J. B54, 299-307, (2006);V. N. Golovach et al. , Phys. Rev. B83, 075401 (2011) ; M. Pierre, M. Hofheinz, X. Jehl, M. Sanquer, G. Molas, M. Vinet, European Phys. J. B 70, 475 (2009)].*

We note that our Silicon SETs are relatively immune to other offset charges because of the screening by the wrapping gate. Offset charges have been identified for a long time as limiting SET applications.

IMPACT OF VARIABILITY

The main identified cause of variability is extrinsic and located in the junction area between the nano-object (here the nanowire silicon channel) and the contacts (here the doped source and drain). This cause will exist in any nano-scale object, whatever its uniformity and cleanliness -once it is contacted to imperfect electrodes. Therefore the main issue to address the variability of nanodevices is to build better electrode junctions. Using high mobility materials such as graphene and carbon nanotubes or bottom-up approaches with chemically perfect channel cannot help if the problem of contact junctions is not addressed properly. This is particularly important for nanoFETs where short SD distance (small delay time) makes the contact junctions very intrusive.

SOLUTIONS?

We can solve this problem

i) by making very clean junctions -in our case by using steeper dopant concentration gradients or Schottky contacts

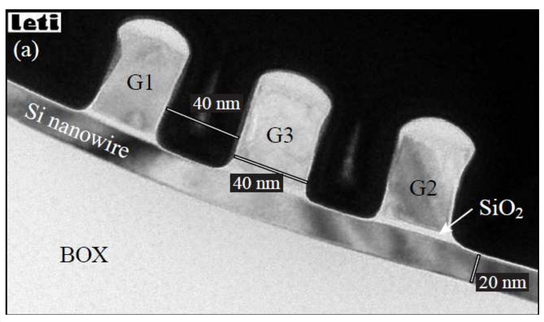
ii) by using junction-less devices -for instance devices consisting in several switches in series (logic-on-a-wire)

iii) by adopting novel fault tolerant logic and computation architectures.

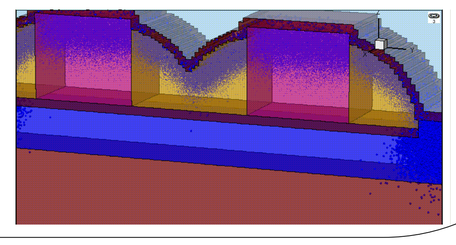
Option i) is actively pursued in main stream CMOS research and our SiSETs will soon benefit from these improvements. Note that the concentration gradients in our current devices are already as sharp as 1 decade/5 nm. NiSi Schottky barrier MOSFETs are also under investigation.

Option ii) is illustrated in figure below where a single undoped SOI nanowire is covered by several gates in series. The SD are located only at the ends of the NW which is protected from implantation by the nitride spacers. Such an arrangement can be used to implement new functionalities beyond the simple switch, as for instance electron pumps, coherent adiabatic transfer, molecular states as charge qubit, ...

Option iii) is out of the scope of this short contribution. A good example- compatible with our mass production of Silicon SETs- can be found in ref *:T. Shibata, Solid-State Electronics 53, 1227 (2009)].*



TEM micrograph of a SOI nanowire covered by 3 polySi gates (pitch 80nm). Coherent or sequential transfer of electrons along the NW is possible by applying appropriate gate voltages [M. Pierre, et al. , Applied Phys. Lett. 95, 242107 (2009)]. During these transfers electrons do not hit any junction with HDD source or drain.



Process Simulation (O. Cueto):no dopant in the SOI covered by spacers