TRAMS PROJECT*:
Terascale Reliable Adaptive Memory Systems
Variability and Reliability of RAM memories in sub-22nm bulk-CMOS technologies

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ABSTRACT

The TRAMS (Terascale Reliable Adaptive MEMORY Systems) project addresses in an evolutionary way the ultimate CMOS scaling technologies and paves the way for revolutionary, most promising beyond-CMOS technologies. We observe significant variability levels of future 18 and 13nm device bulk-CMOS technologies as well as its dramatic effect on the yield of memory cells and circuits. The comparison with one of the promising alternative technologies, Carbon Nanotubes, is also addressed.

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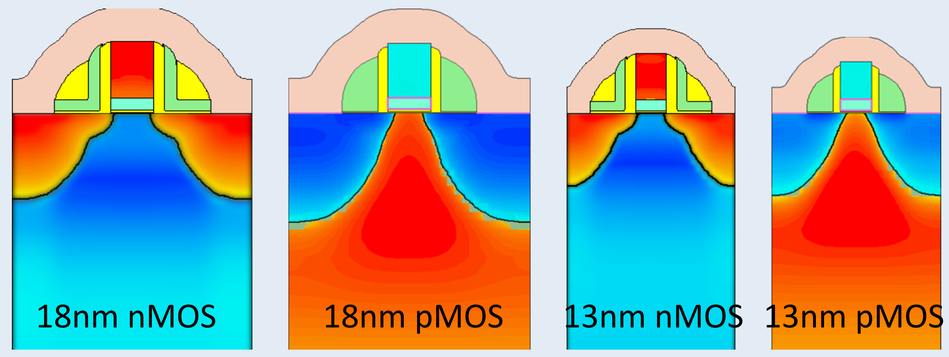
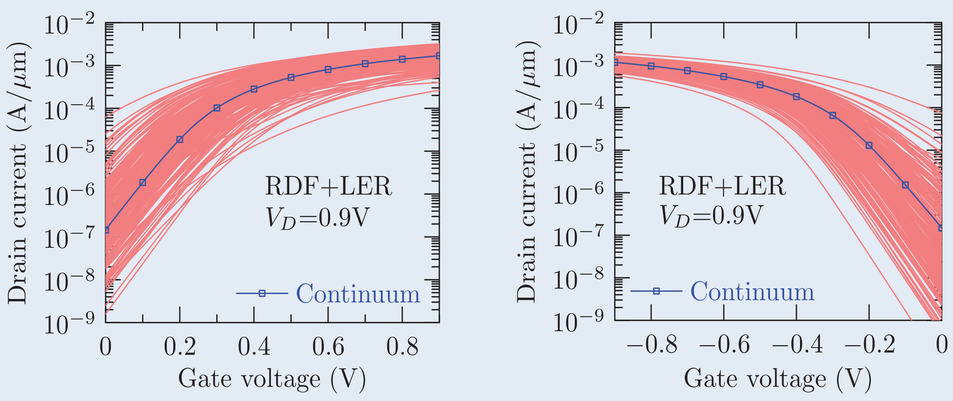
Device Design



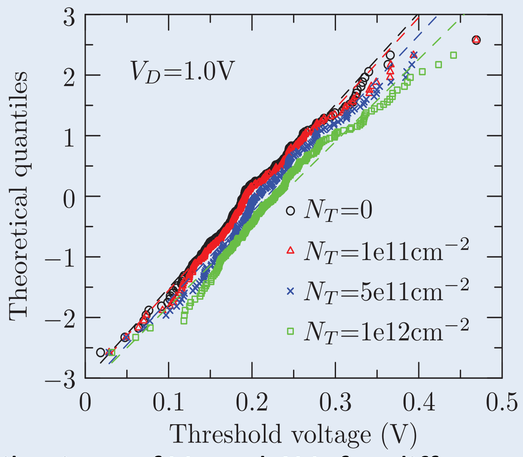
Device structures from process simulation

Statistical Variability Simulations

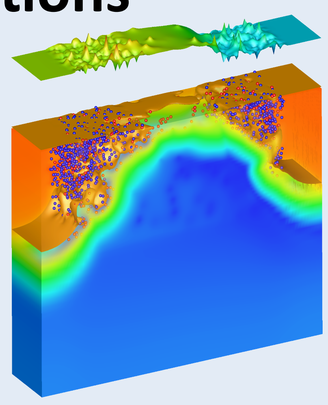


I_D-V_G characteristics for devices with random dopants and LER

Statistical Reliability Simulations

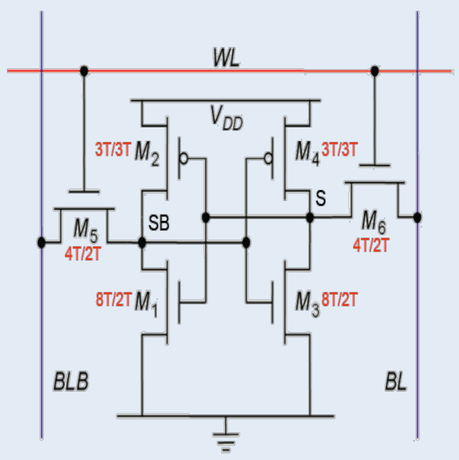


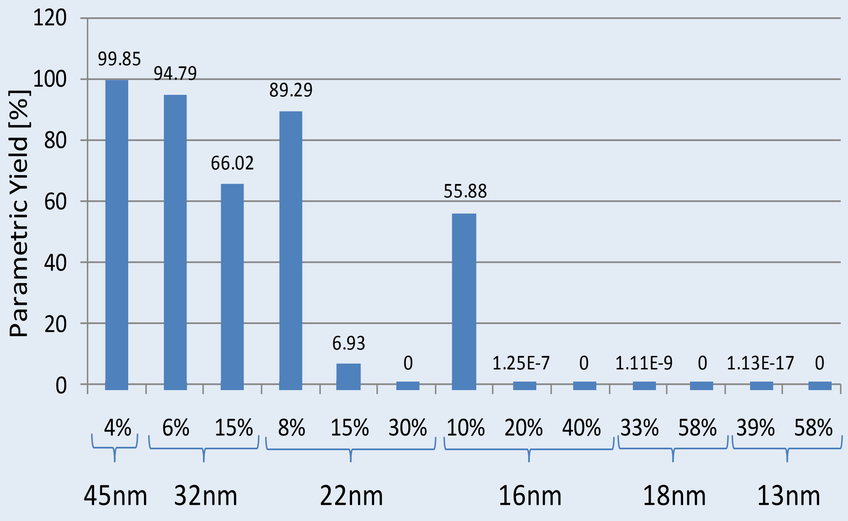
Distributions of V_T and ΔV_T for different trap densities



Trapped charges can block current percolation paths

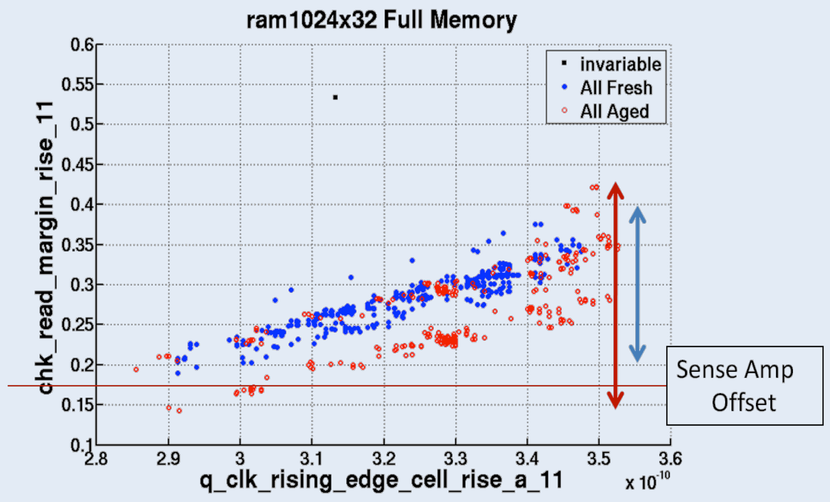
Impact on yield for 6T SRAM





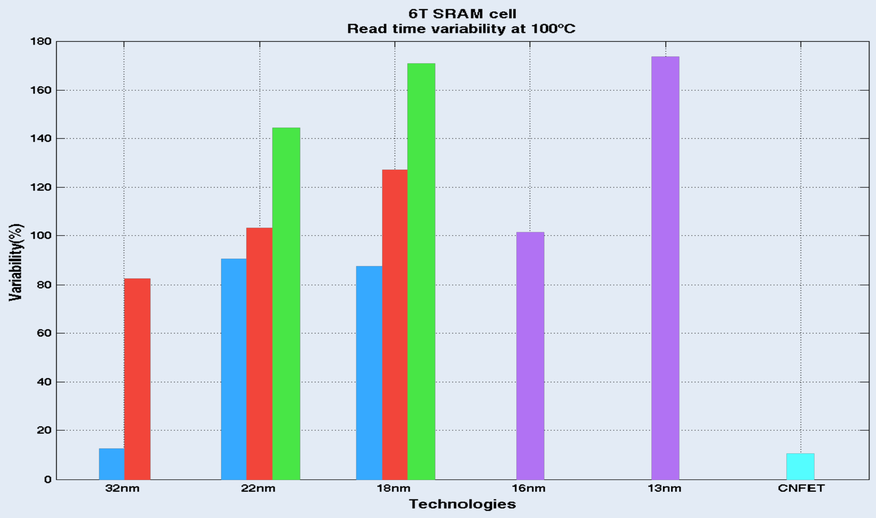
Yield for a 6T SRAM (W/L=1) for different technologies

Aging effects



Timing spread after injecting aged transistors Into the bitcells

Carbon Nanotube Technology



CONCLUSIONS

1. Unexpectedly large variability in the on-current of aggressively scaled MOSFET, due to RDD in source/drain extensions. Electrostatic in its origin and captured by drift-diffusion simulations.
2. Dramatic drop of yield for the 6T SRAM cell under the variability levels determined in TRAMS for 18 and 13 nm, as well as for the PTM technologies considering high and very high variability scenarios.
3. New innovative and aggressive mitigating and adaptive circuitry mechanisms, as well as, redundant and fault tolerant are required in memory systems for sub-22nm technologies. This is the objective of TRAMS project.
4. CNTFET technologies are a sign of hope for future memories implemented in emerging technologies (CNTFETS and presumably others): similar speed and cell area as bulk-16nm SRAM cells but lower leakage and higher yield.

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